N-Channel 2.5-V (G-S) Battery Switch, ESD Protection

PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
28	0.033 at V_{GS} = 4.5 V	4.6
	0.038 at V_{GS} = 3.0 V	4.3
	0.042 at V_{GS} = 2.5 V	4.1

FEATURES

- **Halogen-free**
- Low $R_{DS(on)}$
- V_{GS} Max Rating: 14 V
- Exceeds 2 kV ESD Protection
- 28 V V_{DS} Rated
- Symmetrical Voltage Blocking (Off Voltage)

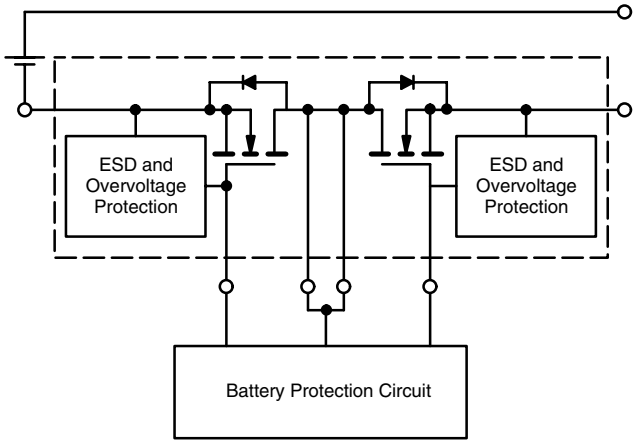
Pb-free

RoHS
COMPLIANT

DESCRIPTION

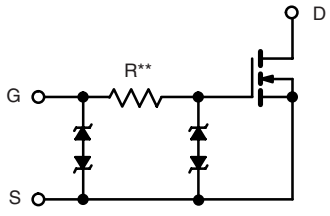
The Si6924AEDQ is a dual N-Channel MOSFET with ESD protection and gate over-voltage protection circuitry incorporated into the MOSFET. The device is designed for use in Lithium Ion battery pack circuits. The common-drain construction takes advantage of the typical battery pack topology, allowing a further reduction of the device's on-resistance. The 2-stage input protection circuit is a unique design, consisting of two stages of back-to-back zener diodes separated by a resistor. The first stage diode is designed to absorb most of the ESD energy. The second stage diode is designed to protect the gate from any remaining ESD energy and over-voltages above the gates inherent safe operating range. The series resistor used to limit the current through the second stage diode during over voltage conditions has a maximum value which limits the input current to ≤ 10 mA at 14 V and the maximum t_{off} to 12 µs. The Si6924AEDQ has been optimized as a battery or load switch in Lithium Ion applications with the advantage of both a 2.5 V $R_{DS(on)}$ rating and a safe 14 V gate-to-source maximum rating.

APPLICATION CIRCUITS



*Thermal connection to drain pins is required to achieve specific performance

Figure 1. Typical Use In a Lithium Ion Battery Pack

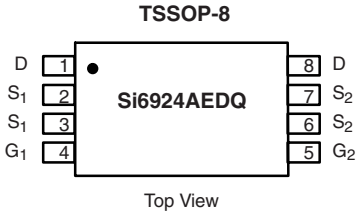


**R typical value is 3.3 kΩ by design.

See Typical Characteristics,
Gate-Current vs. Gate-Source Voltage, Page 3.

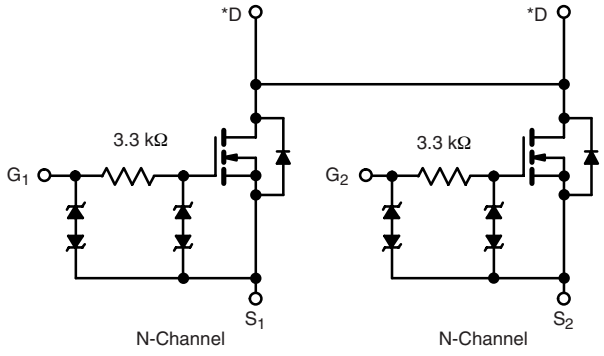
Figure 2. Input ESD and Overvoltage Protection Circuit

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Ordering Information: Si6924AEDQ-T1-GE3 (Lead (Pb)-free and Halogen-free)

Figure 3.



*Thermal connection to drain pins is required to achieve specific performance.

Figure 4.

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted					
Parameter		**Symbol**	**10 s**	**Steady State**	**Unit**
Drain-Source Voltage, Source-Drain Voltage		V_{DS}	28		V
Gate-Source Voltage		V_{GS}	± 14		
Continuous Drain-to-Source Current (T_J = 150 °C)[a]	T_A = 25 °C	I_D	4.6	4.1	A
	T_A = 70 °C		3.7	3.2	
Pulsed Drain-to-Source Current		I_{DM}	20		
Pulsed Source Current (Diode Conduction)[a]		I_S	1.2	0.9	
Maximum Power Dissipation[a]	T_A = 25 °C	P_D	1.3	1.0	W
	T_A = 70 °C		0.84	0.64	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[a]	t ≤ 10 s	R_{thJA}	71	95	°C/W
	Steady State		96	125	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	56	70	

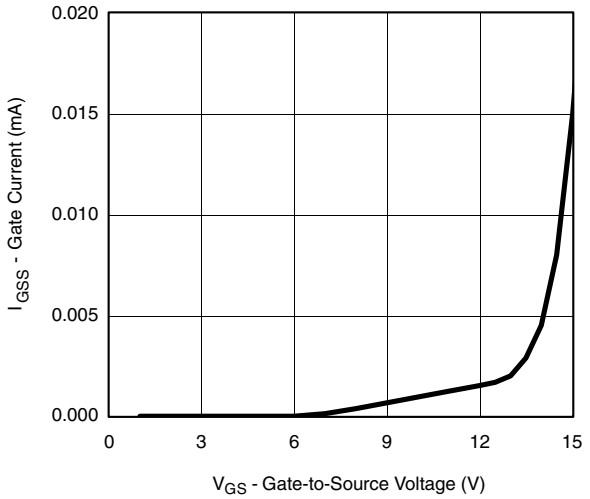
Notes:
a. Surface Mounted on FR4 board.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu A$	0.6		1.5	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 4.5$ V			± 1	µA
		$V_{DS} = 0$ V, $V_{GS} = \pm 14$ V			± 20	mA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 22.4$ V, $V_{GS} = 0$ V			1	µA
		$V_{DS} = 22.4$ V, $V_{GS} = 0$ V, $T_J = 55$ °C			5	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 5$ V	10			A
Drain-Source On-State Resistance[b]	$R_{DS(on)}$	$V_{GS} = 4.5$ V, $I_D = 4.6$ A		0.022	0.033	Ω
		$V_{GS} = 3.0$ V, $I_D = 4.3$ A		0.025	0.038	
		$V_{GS} = 2.5$ V, $I_D = 4.1$ A		0.029	0.042	
Forward Transconductance[b]	g_{fs}	$V_{DS} = 10$ V, $I_D = 4.6$ A		25		S
Diode Forward Voltage[b]	V_{SD}	$I_S = 1.2$ A, $V_{GS} = 0$ V		0.7	1.1	V
Dynamic[a]						
Total Gate Charge	Q_g	$V_{DS} = 10$ V, $V_{GS} = 4.5$ V, $I_D = 4.6$ A		6.5	10	nC
Gate-Source Charge	Q_{gs}			1.2		
Gate-Drain Charge	Q_{gd}			1.5		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10$ V, $R_L = 10\ \Omega$ $I_D \cong 1$ A, $V_{GEN} = 4.5$ V, $R_G = 6\ \Omega$		0.95	1.5	µs
Rise Time	t_r			1.4	2.1	
Turn-Off Delay Time	$t_{d(off)}$			7	11	
Fall Time	t_f			3.1	5	

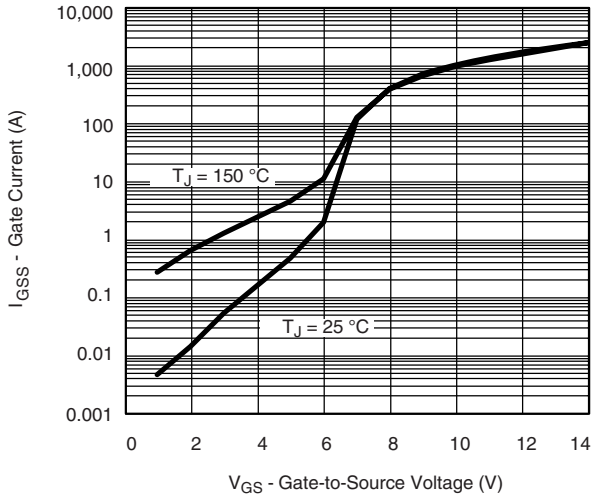
Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

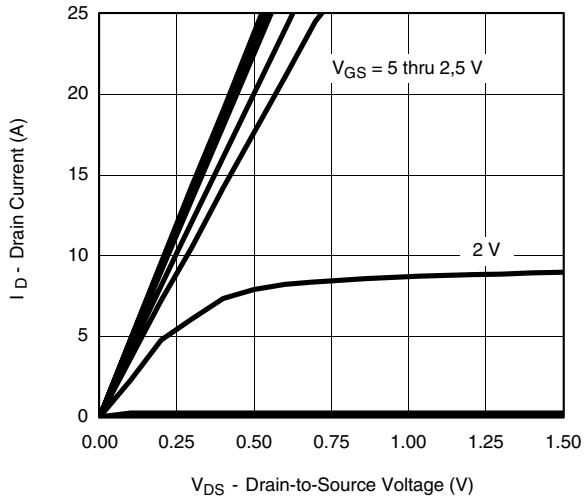


Gate-Current vs. Gate-Source Voltage

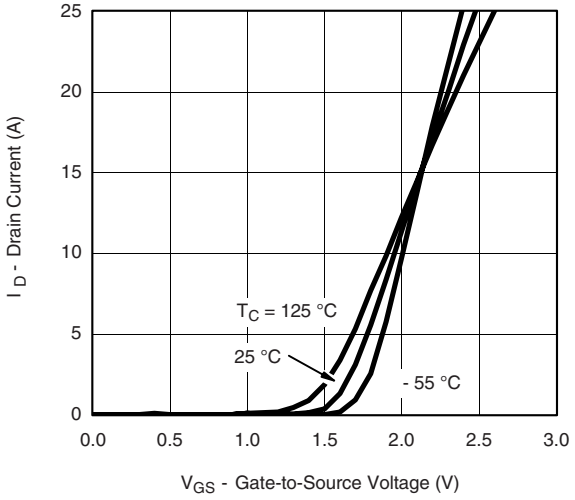


Gate Current vs. Gate-Source Voltage

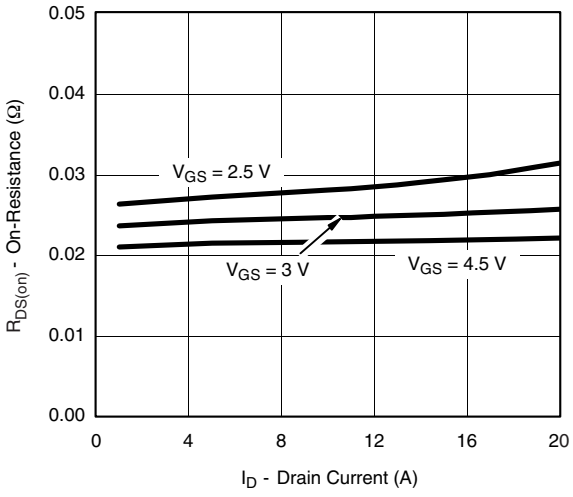
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



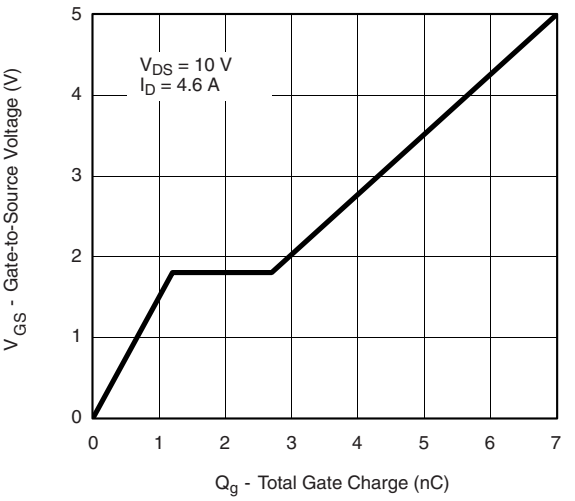
Output Characteristics



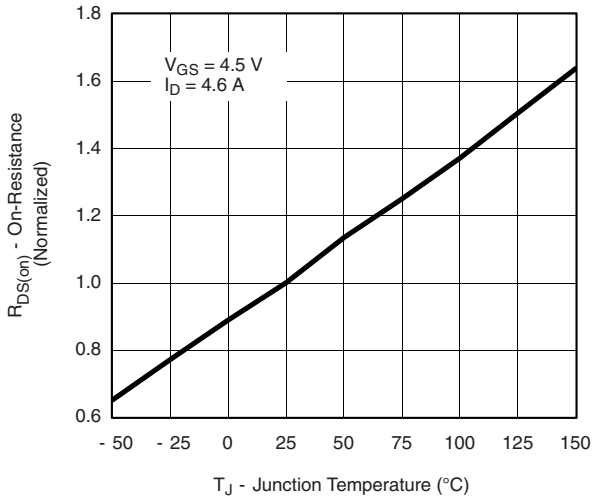
Transfer Characteristics



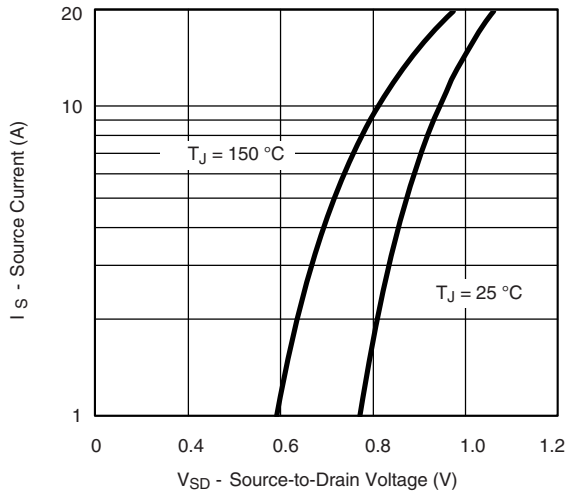
On-Resistance vs. Drain Current



Gate Charge

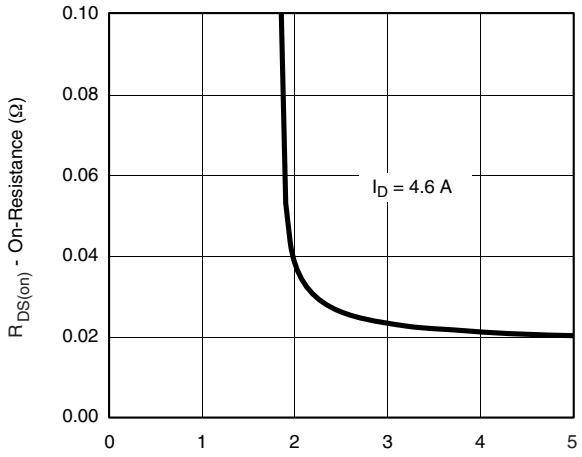


On-Resistance vs. Junction Temperature

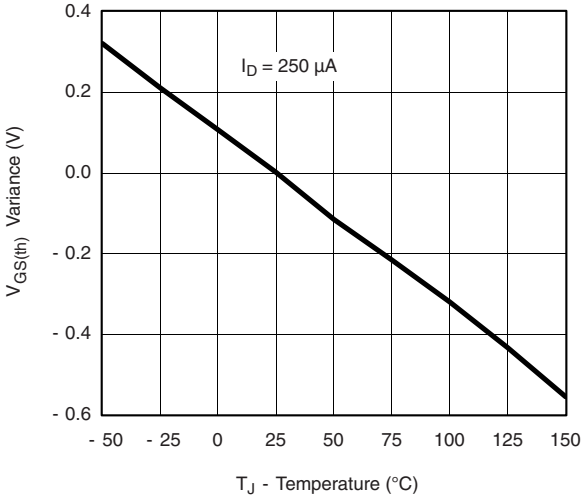


Source-Drain Diode Forward Voltage

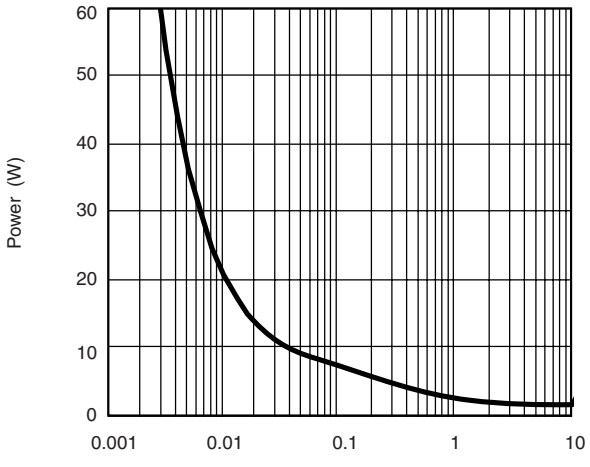
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



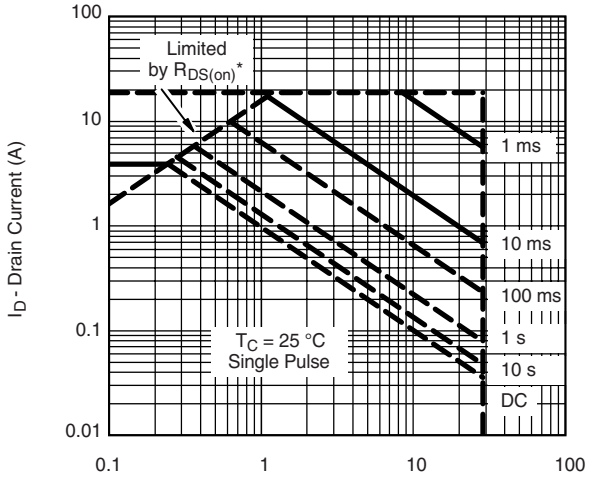
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

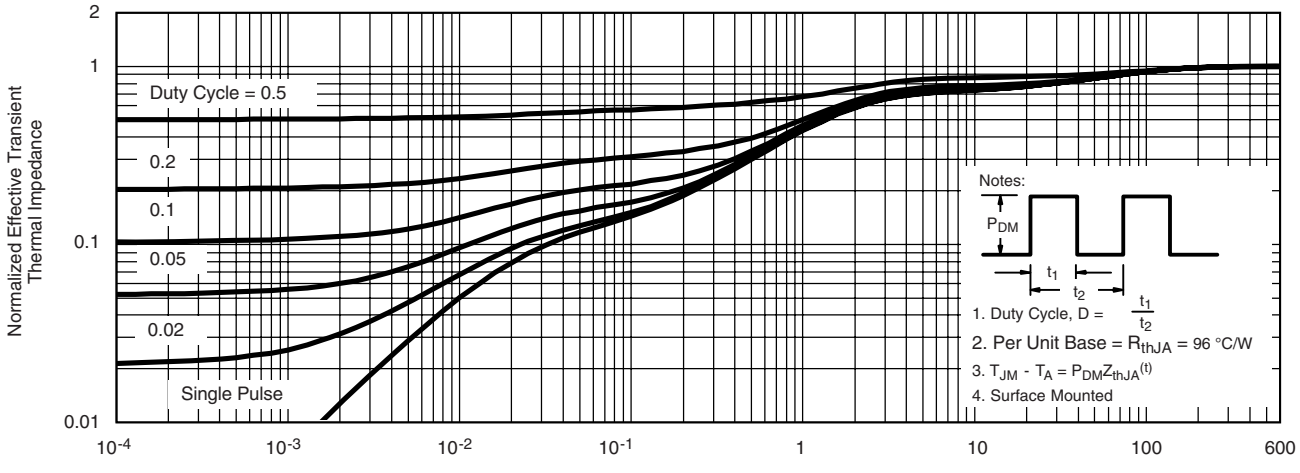


Single Pulse Power



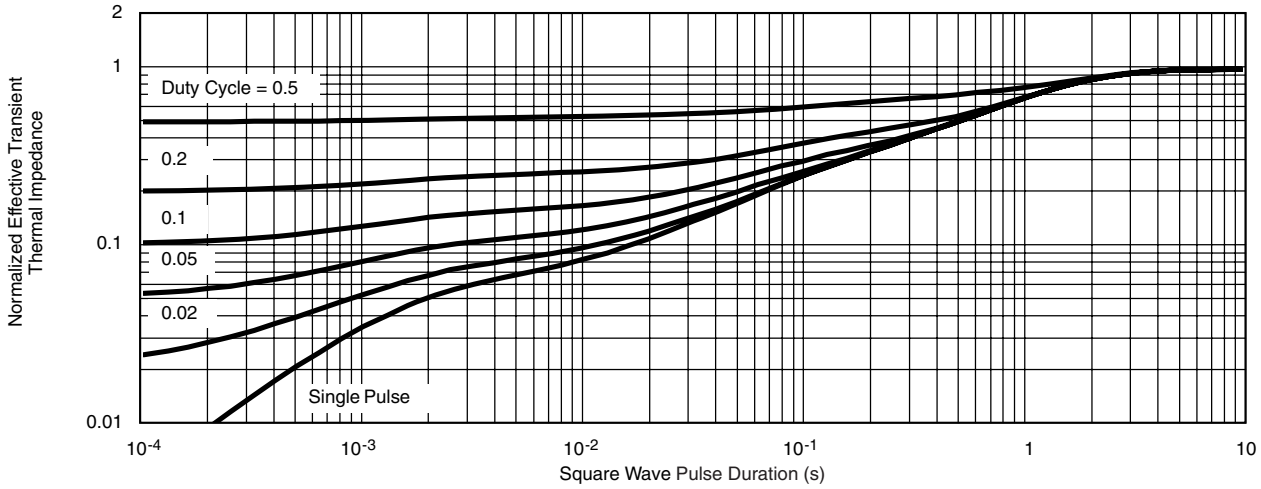
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?72215.

Disclaimer

All product specifications and data are subject to change without notice.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, “Vishay”), disclaim any and all liability for any errors, inaccuracies or incompleteness contained herein or in any other disclosure relating to any product.

Vishay disclaims any and all liability arising out of the use or application of any product described herein or of any information provided herein to the maximum extent permitted by law. The product specifications do not expand or otherwise modify Vishay’s terms and conditions of purchase, including but not limited to the warranty expressed therein, which apply to these products.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications unless otherwise expressly indicated. Customers using or selling Vishay products not expressly indicated for use in such applications do so entirely at their own risk and agree to fully indemnify Vishay for any damages arising or resulting from such use or sale. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

Product names and markings noted herein may be trademarks of their respective owners.